

Generation and motion of dislocations in silicon wafers subjected to multi-step annealing

This article has been downloaded from IOPscience. Please scroll down to see the full text article.

2002 J. Phys.: Condens. Matter 14 12909

(<http://iopscience.iop.org/0953-8984/14/48/332>)

View [the table of contents for this issue](#), or go to the [journal homepage](#) for more

Download details:

IP Address: 171.66.16.97

The article was downloaded on 18/05/2010 at 19:14

Please note that [terms and conditions apply](#).

Generation and motion of dislocations in silicon wafers subjected to multi-step annealing

M V Mezhennyi¹, M G Mil'vidskii¹, V Ya Reznik¹ and R J Falster²

¹ Institute of Rare Metals, Moscow, Russia

² MEMC Electronic Materials SpA, Novara, Italy

E-mail: icpm@mail.girmet.ru (M V Mezhennyi)

Received 27 September 2002

Published 22 November 2002

Online at stacks.iop.org/JPhysCM/14/12909

Abstract

Peculiarities of the dislocation generation and propagation in Cz silicon wafers after various heat treatments have been studied by the four-point-bending method. It was shown that heat treatment strongly influenced the mechanical properties of the wafers. Annealing at 450 °C leads to substantial strengthening of the wafers in comparison with the as-grown state. Multi-step annealing in regimes of intrinsic getter formation in wafers causes substantial decrease of the critical stresses for generation of dislocations and increase of their mobility. It was shown that both oxygen precipitates and precipitate–dislocation clusters that formed in the wafer bulk during the multi-stage thermal treatments are effective centres of heterogeneous generation of dislocations by thermal or mechanical stresses.

1. Introduction

Currently, the following problems are main focuses of research attention:

- (1) the mechanical strength of monocrystalline dislocation-free silicon wafers,
- (2) the nature of centres for heterogeneous generation of dislocations in them,
- (3) factors determining dynamical properties of generating dislocations [1–5].

There are at least two reasons for this. On the one hand, the tendency of the crystal diameter to increase leads to substantial increase of the dislocation generation probability in wafers during high-temperature processes of device formation due to both thermal stress increase and wafer weight increase. On the other hand, in modern ULSI manufacturing technology, wafers with the intrinsic getter created by controlled decomposition of supersaturated oxygen solid solution are used. Depending on their nature and size, oxygen precipitates in the wafer bulk can play the role of centres for heterogeneous generation of dislocations as well as barriers to dislocation motion and, therefore, hamper dislocation generation and propagation [6, 7]. The

Table 1. Regimes of silicon wafer multi-stage thermal treatment.

Lot number	Thermal treatment regime
1	As grown
2	1000 °C/15 min + 450 °C/16 h
3	1000 °C/15 min + 650 °C/16 h
4	1000 °C/15 min + 450 °C/16 h + 800 °C/4 h + 1000 °C/4 h
5	1000 °C/15 min + 650 °C/16 h + 800 °C/4 h + 1000 °C/4 h

aim of this investigation is to study the influence of multi-stage thermal treatments designed for intrinsic getter formation on dislocation dynamical properties in silicon wafers.

2. Samples for investigation and experimental methods

Samples were cut from ‘vacancy-type’ {100} wafers of 150 mm diameter, dislocation-free Cz single crystal. The concentration of oxygen in the sample was $(7-8) \times 10^{17} \text{ cm}^{-3}$; the resistivity was $-1-5 \text{ } \Omega \text{ cm}$. The wafers investigated were as-grown samples and samples following various multi-stage thermal treatments including a regime of intrinsic getter formation (the thermal treatment regimes are presented in table 1).

The samples for the mechanical tests were in the form of parallelepipeds ($25 \times 4 \times 0.6 \text{ mm}^3$) with a {100}-oriented large side, and (100)-oriented long edges. The samples were chemically polished in a HF:HNO₃ = 1:6 mixture for 5 min. A surface layer of thickness about 40 μm was removed during this treatment. Then several marks were made on the {100} surface investigated with a Knoop indenter (the indenter load was 0.25 N; the loading time was 15 s). After that, the sample was placed in the four-point-bending machine [8]. The mechanical tests were carried out at temperatures of 600–800 °C. To reduce the influence of transient processes caused by sample heating and cooling, the sample was located in a furnace already heated up to the given temperature, and after loading the sample was removed from the machine and quenched in the air. The sample heating time up to the test temperature was less than 5 min. The time under load was 20 min. At loading, the sample side with the indenter marks was stretched. Sample subsurface layer dislocation semi-loops originated from sample surface indentation and further loading at the test temperature. They consist of two 60° segments and screw dislocation fragments parallel to the sample surface. In our case, at impact of the bend stresses along the [110] direction, four dislocation slip systems are activated relative to the bend axis $[1\bar{1}0]$: (111) $[\bar{1}01]$; (111) $[0\bar{1}1]$; $(\bar{1}\bar{1}1) [0\bar{1}\bar{1}]$; and $(\bar{1}\bar{1}1) [101]$. The mobility of the 60° dislocation loop segments was studied in the investigations.

Stresses causing dislocation generation from internal sources in the wafer bulk were identified by the onset of the mass generation of the dislocations not relating to indenter marks. In these cases, after selective chemical etching, numerous slips at the sample surface and sample macrobending were revealed.

The mechanisms of dislocation generation and propagation in silicon samples were investigated by the optical microscopy method, x-ray diffractometry and topography, and transmission electron microscopy (TEM). For investigations by the optical microscopy method, the samples were processed in the selective etchant HF:0.15 M CrO₃ = 1:1.

3. Results of investigations

In all starting samples, typical defects were microdefects. The density of these microdefects in as-grown samples was about $8 \times 10^5 \text{ cm}^{-3}$. Thermal treatments at 450 and 600 °C (sample

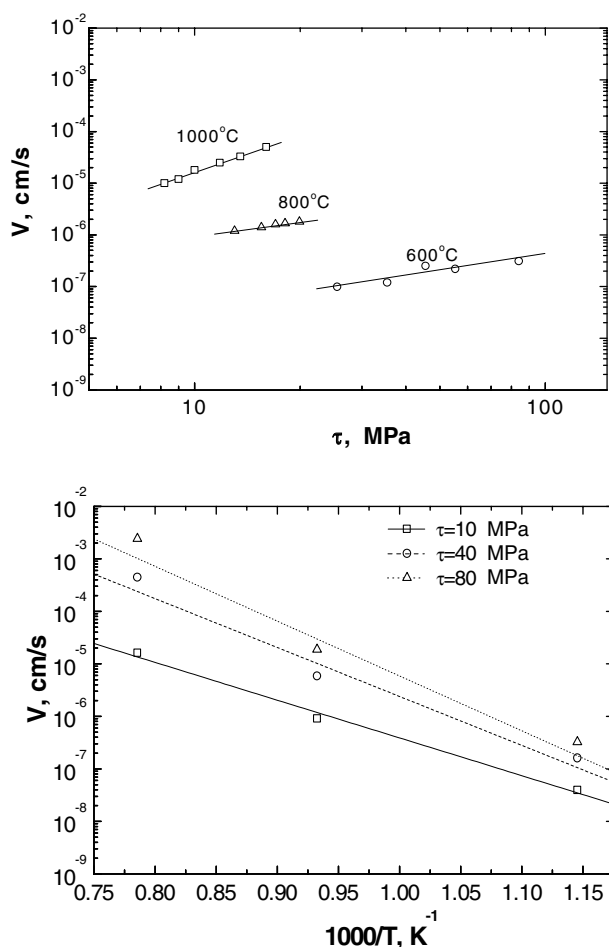


Figure 1. The dependence of the 60° dislocation velocity on the applied shear stress (a) and the temperature dependence of the dislocation velocity for several values of the shear stress (b) for samples of lot 1.

lots 2 and 3) did not result in substantial change of the microdefect density being revealed. Multi-stage thermal treatments in regimes of intrinsic getter formation (sample lots 4 and 5) caused drastic increases of the microdefect density—up to 10^{11} cm^{-3} according to TEM data.

In figure 1 the dependences of the dislocation propagation velocity on the shear stresses and temperature for as-grown samples (lot 1) are presented. In the stress and temperature ranges investigated, the data obtained are satisfactorily described by the well-known equation [1]

$$V = V_0(\tau/\tau_0)^n \exp[-E/kT] \quad (1)$$

where: V is the dislocation propagation velocity; V_0 is the crystal matrix state constant; τ_0 is a constant (1 MPa); n is the magnitude of the degree; E is the activation energy for dislocation propagation.

The activation energy value calculated from the data presented is 1.8 eV. It should be noted that the dislocation propagation induced by indenter marks begins upon some critical level of stress being exceeded. We will refer to this value as the critical stress of dislocation loop propagation onset, τ_{cr} .

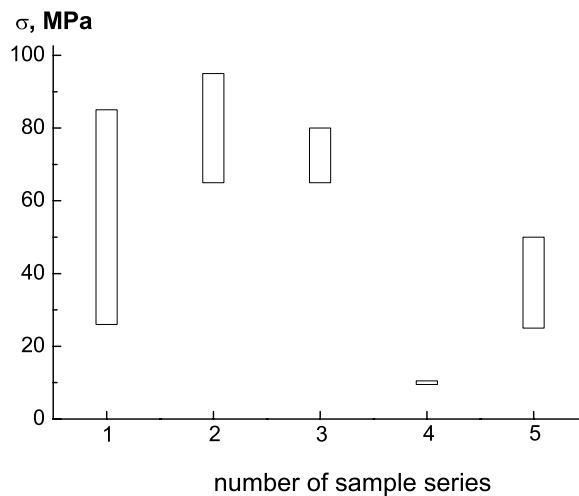


Figure 2. The dependence of the 60° dislocation velocity on the applied shear stress for the samples of lots 2, 3, and 5 (loading at 600 °C).

We shall denote the stress at the onset of dislocation generation from internal sources in the volume of a sample as τ_{pi} . In our case, τ_{cr} is a stress value which causes propagation of dislocation loops with minimal size. The optical microscope ‘Polyvar’, used in our experiments, allows one to distinguish easily loops with size of about 3 μm . As follows from the data presented (figure 1), the τ_{cr} -value decreases substantially with temperature increase.

In figure 2, the dependence of the propagation velocity of the indenter-induced dislocation on the stress values at 600 °C is shown for sample lots 2, 3 and 5. It should be noted that for samples after multi-stage thermal treatment in the intrinsic getter formation regimes, the τ_{cr} -value is substantially lower than that for samples after low-temperature thermal treatment (lots 2 and 3). The dislocations in the samples of lot 5 have high mobility at substantially lower shear stresses. At stress values higher than 40 MPa, mass dislocation generation induced by internal sources has been observed in these samples. It substantially complicates the observation of propagation of indenter-induced dislocation. The same phenomenon has been observed for the samples of lot 2 at stress values higher than 95 MPa, and for the samples of lot 3 at stress values higher than 80 MPa.

In sample lot 4, mass generation of dislocations induced by internal sources has been observed at shear stress values lower than 10 MPa, while dislocations induced by indenter marks were still not movable. Because of this, it is impossible to study the dependence of the dislocation propagation velocity on the applied stress values for the samples of the given lot. For temperature increase up to 800 °C, similar phenomena have already been observed in sample lots 3 and 5. This makes it impossible to define the dislocation propagation velocity in these samples at the given temperature. It should be noted that the dislocation generation induced by internal sources in samples immediately after growth (lot 1) started at substantially higher shear stresses than that in the samples that had undergone thermal treatment. That allows us to investigate the dislocation mobility at temperatures up to 1000 °C (figure 1). Samples of lot 2 were exceptions—at 600 and 800 °C, both the τ_{cr} -values and the stress values for dislocation generation induced by internal sources were substantially lower than those for as-grown samples. For sample lot 3 at 800 °C, these values were comparable.

The histogram characterizing the behaviour of the samples investigated during the mechanical tests at 600 °C is presented as figure 3. In the histogram the lower boundaries

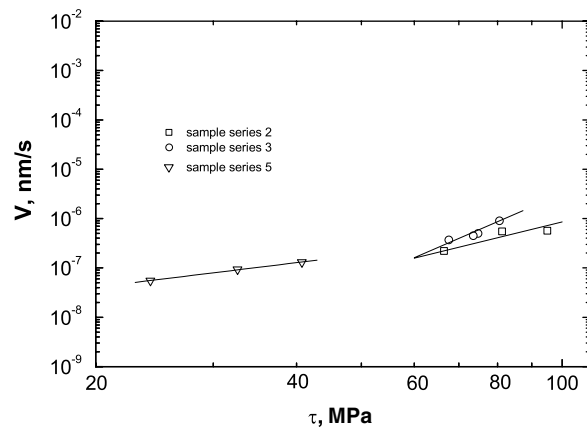
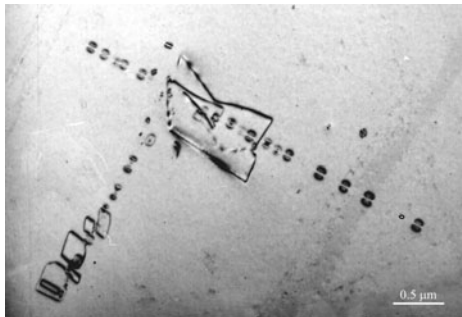


Figure 3. The histogram for distributions of τ_{cr} (the lower boundaries of corresponding columns indicate these values) and τ_{pl} (the upper boundaries) in different series of samples (loading at 600 °C).

(a)



(b)

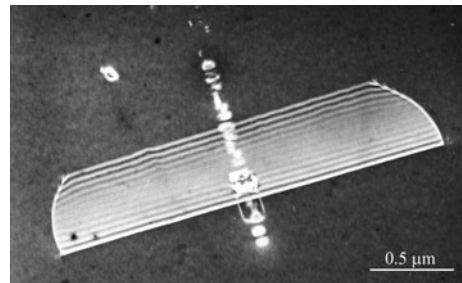


Figure 4. TEM images of typical defects found after mechanical tests: (a) a chain of precipitates and loops along the [110] direction forming around an initial precipitate (bright field, $g = 220$, $s > 0$); (b) an initial stacking fault of interstitial type and a chain of precipitates and loops (dark field, $g = 220$, $s < 0$) forming during mechanical testing.

of the corresponding columns denote τ_{cr} -values and the upper boundaries denote stresses causing mass dislocation generation induced by internal sources. Thermal treatments at low temperature (450 and 650 °C) for 16 h lead to substantial increase in the τ_{cr} -value in comparison with that for as-grown samples. Multi-stage thermal treatment in the intrinsic getter formation regime (lots 4 and 5) leads to substantial wafer ‘softening’. In view of this, the regime of four-stage thermal treatment including a low-temperature (450 °C) stage (sample lot 4) is especially problematic. For lot 5, the τ_{cr} -values were comparable with values which are characteristic for as-grown samples. At the same time, mass dislocation generation induced by internal sources started in the samples of lot 5 at substantially lower stress values.

By means of TEM investigations of samples after mechanical tests, it was shown that oxygen precipitates are centres of heterogeneous generation of dislocations in wafer bulk. These precipitates are formed as a result of supersaturated oxygen solid solution decomposition during thermal treatment designed for intrinsic getter formation in wafers. Dislocation loops forming around precipitates propagate in wafer bulk by the ‘prismatic extrusion’ mechanism (figure 4).

4. Discussion

The results obtained show that low-temperature thermal treatment at 450 °C for 16 h leads to substantial strengthening of wafers in comparison with as-grown ones. This is confirmed by increases of both τ_{cr} -values and τ_{pl} -values. Also it is confirmed by the decrease of the dislocation propagation velocity due to external stresses. For increase of the temperature of the low-temperature annealing to 650 °C, the τ_{cr} -value for the wafers remains higher than that for as-grown samples. However, τ_{pl} has lower values.

Multi-stage thermal treatment in the regime of intrinsic getter formation in wafer bulk leads to weakening of wafers. The most abrupt weakening (in comparison with as-grown samples) was observed when the low-temperature stage of the multi-stage annealing was performed at 450 °C (lot 4). For such wafers, the τ_{cr} -values and τ_{pl} -values are comparable and several times lower than those for as-grown wafers. This lot of wafers also have the poorest crystal perfection among all of the samples investigated. At the low-temperature (650 °C) stage, the multi-stage thermal treatments were not so harmful— τ_{cr} -values for these wafers, although lower, were comparable with the corresponding values for as-grown wafers, and dislocation mass generation stress values induced by internal sources reduced only from ~ 85 to 50 MPa (sample lot 5).

The main reason for the observed phenomenon is, probably, silicon lattice structural change which is caused by supersaturated oxygen solid solution decomposition during thermal treatment of the wafers. It is well known that thermal treatment at 450 °C leads to generation of thermodonors which are clusters consisting of a few oxygen atoms. The concentration of such clusters can reach 10^{16} cm^{-3} and they are probably effective barriers hampering the dislocation loop origination and propagation in the crystal matrix caused by the external load. An annealing temperature increase to 650 °C leads to enlargement of the oxygen clusters formed. At the same time, together with the fine clusters, which are barriers to loop motion, in the lattice there are enlarged oxygen precipitates which are centres of heterogeneous generation of dislocations. Thus, after such annealing, τ_{cr} -values of wafers remain at a reasonably high level, and the τ_{pl} -values become comparable with those of as-grown wafers.

During multi-stage (in our case four-stage) thermal treatments of wafer bulk, a large amount of fairly big precipitates and precipitate–dislocation clusters are formed. These clusters act as a getter for fast-diffusing contaminations. As shown by TEM, the concentration of these centres in wafers reaches $(1\text{--}4) \times 10^{11} \text{ cm}^{-3}$. Plate-like precipitates with size ~ 150 nm are formed in wafers where the low-temperature stage has been performed at 450 °C. The size of the precipitates formed is about 220 nm for wafers where the low-temperature stage has been performed at 650 °C. The thicknesses of these precipitates are up to ~ 100 nm. At the same time, there are precipitates with much smaller sizes in the lattice. Sufficiently big precipitates can act as effective centres of heterogeneous generation of dislocations caused by thermal or mechanical stresses.

During the mechanical tests of wafers with intrinsic getters, dislocation loops are in our case generated around precipitates. These loops are located in the precipitate habit plane. Then, these loops nonconservatively creep up in a slip plane and propagate in the crystal matrix by the prismatic extrusion mechanism (figure 5(a)). In another case, the balls of dislocation loops are formed around precipitates. Some of them are located in corresponding slip planes. At the same time, fine precipitates located in the crystal matrix are barriers to the loops (figure 5(b)). The difference between the defect states which are formed in the crystal lattice during multi-stage thermal treatment of the samples of lots 4 and 5 is, probably, the main reason for such substantial differences between their strength characteristics. The results obtained demonstrate the importance of the correct selection of low-temperature annealing temperature–time regimes. It is the low-temperature annealing at 650 °C that gives indubitable advantages.

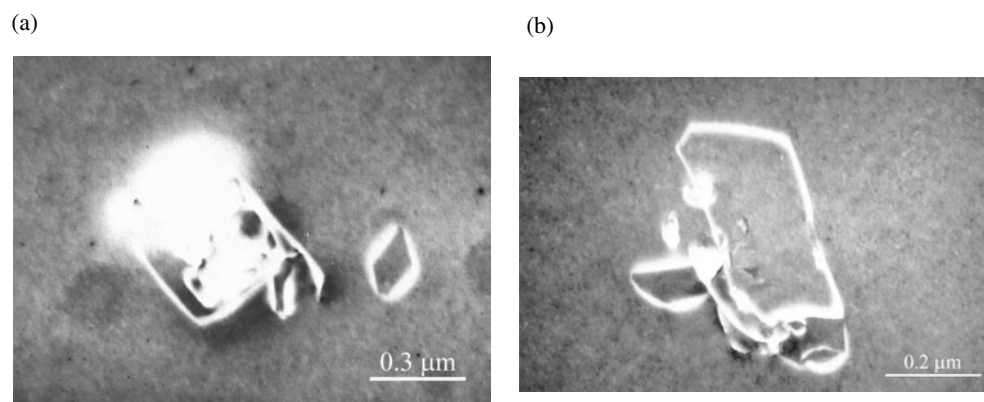


Figure 5. TEM images of typical defects formed by different generation mechanisms: (a) the initial stage of prismatic punching, an oxygen precipitate, and dislocation loops (dark field, $g = 220$, $s < 0$); (b) a particle surrounded by a 3D dislocation entanglement (dark field, $g = 220$, $s < 0$).

5. Conclusions

Peculiarities of dislocation generation and propagation in Cz silicon wafers after various heat treatments have been studied by the four-point-bending method. It was shown that annealing wafers at 450 °C leads to substantial strengthening in comparison with as-grown ones. It has been assumed that the oxygen clusters formed during such thermal treatment are effective barriers to formation and propagation of dislocation loops. Substantial wafer weakening after multi-stage thermal treatment in intrinsic getter formation regimes has been revealed. It was shown that both oxygen precipitates and precipitate–dislocation clusters formed in wafer bulk during multi-stage thermal treatment are effective centres of heterogeneous generation of dislocations by thermal or mechanical stresses. It has been established that the temperature–time regimes of the low-temperature stage during defect state formation takes a substantial role in determining the matrix of the silicon lattice and the wafer strength characteristics.

Acknowledgments

This work has been supported by a grant from the Russian fund for basic research, No 02-02-16053A.

References

- [1] Alexander H 1986 *Dislocations in Solids* vol 7, ed F R N Nabarro (Amsterdam: Elsevier) ch 35, pp 113–235
- [2] Sumino K 1985 *Proc. 1st Int. Autumn School on Gettering and Defect Engineering in Semiconductor Technology (Garzau)* ed H Richter (Zürich: Scitec Publications) p 41
- [3] Senkader S, Jurkschat K, Gambaro D, Falster R J and Wilshaw P R 2001 *Phil. Mag. A* **81** 759
- [4] Peidous I V and Loiko K V 2000-17 *Electrochem. Soc. Proc. 2000-17* (Pennington, NJ: The Electrochemical Society) p 145
- [5] Peidous I V, Loiko K V, Balasubramaniam N and Schuelke T 2000 *Electrochem. Soc. Proc. 2000-17* (Pennington, NJ: The Electrochemical Society) p 180
- [6] Enisherlova K L, Mil'vidskii M G, Reznik V J and Rusak T F 1991 *Crystallogr. Rep.* **36** 1259
- [7] Mezhenyi M V, Mil'vidskii M G, Pavlov V F and Reznik V J 2001 *Fiz. Tverd. Tela* **1** 47
- [8] Koncevoi Yu A, Litvinov Yu M and Fattahov E A 1982 *Plasticity and Durability of Semiconductor Materials and Structures* (Moscow: Radio and Communication)